UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,294	09/10/2003	Yukiko Iwasaki	03560.002998.1	2455

5514 7590 12/01/2004

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,294	IWASAKI ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-29,33-39 and 59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-29,33-39 and 59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/083,585.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 25 – 29 and 33 – 39 rejected under 35 U. S.C. 103(a) as being unpatentable for reasons of record in Paper No. 12 is reproduced below:

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 25 – 29 and 34 – 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaguchi, US 5,856,229 and Ahn, US 6,274,937 in view of Henley, US 6,548,382 and Lee, US 6,486,008.

Regarding claim 25, Sakaguchi teaches a method for manufacturing a semiconductor film by preparing a first member (see Fig. 2B) including a semiconductor substrate 21, a semiconductor layer 23 and a separation layer 22 provided between the semiconductor substrate 21 and the semiconductor layer 23 in column 7, under Embodiment 2. According to Example 3 in page 12, substrate is Si and the layer 23 is GaAs. The resistivity of GaAs is inherently higher than that of the Si as shown by Ahn in column 3, lines 1 – 3. Sakaguchi teaches separating the semiconductor layer 23 from the semiconductor substrate 21 at the separation layer 22 with reference to Figs 2C – 2 E and Example 3 in column 12 by a pulling force.

Sakaguchi fails to teach separating the layer by heating the first member by induction heating.

Henley and Lee teach a very similar process of separating a semiconductor layer from a substrate by cleaving the porous layer by using an electromagnetic field for induction heating (see Henley in column 8, lines 45 – 48 and Lee in column 5, lines 41 – 50.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Sakaguchi by separating the porous layer by applying induction heating since Henley teaches that controlled cleavage can be initiated in the

porous layer with the help induction heating and Lee teaches the benefit of induction heating by affording even heating in column 5, lines 41 – 50.

Regarding claim 26, Sakaguchi teaches bonding a second member 24 onto the semiconductor layer (see Fig. 2C) before separation.

Sakaguchi fails to teach bonding a second member that is hardy heated by induction heating.

Henley and Lee teach induction heating for cleaving the porous layer and Henley specifically teaches the importance of localized heating instead of the global heating in column 8, lines 60 – 65 and the use of thermal sink in column 8, lines 45 - 56. Henley also teaches that energy can be applied only to the donor wafer (substrate of the first member) in column 8, lines 3 – 5.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Sakaguchi by applying the induction heating in such a way that the heating is localized within the porous area through the first member and not heating the second member (receptor wafer) so that the cleaving action is properly initiated at the intended location as taught by Henley.

Regarding claim 27, Sakaguchi teaches insulative supporting substrate of silicon oxide in column 9, lines 13 – 25.

Henley teaches supporting substrate of dielectric materials in column 6, lines 49 – 56. The dielectric/insulative materials for the second member will inherently have higher resistivity than the first member since the first member is a semiconductor material.

Regarding claims 28 and 29, GaAs will inherently have resistivity higher than 1 Ohm.cm and the Si substrate especially p and n-type substrates will have resistivity in the order of 0.1 Ohm.cm or less.

Regarding claim 34, Sakaguchi fails to disclose forming slits in the separation layer before induction heating.

Henley teaches various ways to initiate the cleaving in column 8, lines 1 – 65, including initiating first cleaving and then sustaining it with other forms of energy.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Sakaguchi by initiating the cleavage by forming crack slits and then apply the heating to sustain the cleavage in order to obtain a defect free separation of the two layers.

Regarding claims 35 and 36, Henley teaches simultaneous application of various energies for the cleaving action throughout column 8 and especially in lines 58 – 60 including the fluid and mechanical forces, which include tensile, compressive and shear forces.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Sakaguchi by initiating the cleavage by simultaneous application of thermal and mechanical or hydrostatic pressure as taught by Henley in order to obtain a defect free separation of the two layers.

Regarding claims 37 – 39, Sakaguchi teaches removing the porous layer residue from the separated layer, separated substrate and reutilization of substrate for

subsequent processing in columns 4 and 5 under the heading "Summary of the Invention".

6. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaguchi, US 5,856,229 and Ahn, US 6,274,937 in view of Henley, US 6,548,382 and Lee, US 6,486,008 as applied to claim 25 above, and further in view of Wada, US 6,222,167.

Sakaguchi and Ahn in view of Henley and Lee teach induction heating but fails to teach heating by mounting the first member on an induction – heating mount around which a coil is wound and causing the current to flow in the substrate by supplying the coil with a high frequency current.

Induction heating is a well-known heating method and Wada shows in Fig. 8 and in column 2, lines 6 – 9 that a coil 7 is wound around the material 8 to be heated by causing the current to flow in the substrate by supplying the coil with a high frequency current.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Sakaguchi by separating the porous layer by using induction heating as taught by Henley and Lee and use the high frequency coil taught by Wada since this is a well-known prior art process for induction heating.

7. Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaguchi, US 5,856,229 and Ahn, US 6,274,937 in view of Henley, US 6,548,382 and Lee, US 6,486,008 as applied to claim 26 above, and further in view of Henley, US 6,033,974 and Linn, US 5,526,768.

Sakaguchi uses the second member 24 as a target substrate by leaving the separated semiconductor film on it but fails to teach separating the second member from the semiconductor layer.

Henley teaches that the second member called a handle wafer 500 is bonded to the first substrate with reference to Fig. 5 for the purpose of easily handling the composite structure in column 8, lines 8 – 18.

Linn teaches that the purpose of the handle wafer is to provide support for handling delicate composite bonded substrate and is finally removed once the desired substrate structure has been successfully separated from the composite bonded structures as illustrated through Figs 1(a) – 1(d), 2(a) – 2(h) and subsequent series of figures and is well known in separating composite bonded substrates.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Sakaguchi and use the second member as a handle wafer that can be later separated to form the semiconductor layer on the insulating intermediate layer to facilitate handling of the composite bonded structure as taught by Henley with reference to Fig. 5 and Linn with reference to Figs. 2(a) – 2(h).

Response to Arguments

8. Applicant's arguments filed October 18, 2004 have been fully considered but they are not persuasive due to the following reasons.

The Applicant's argument is regarding the independent claim 25 featuring the differences of resistivity between the semiconductor substrate and the semiconductor layer with an interposing separation layer and separating the substrate from the

semiconductor layer by induction heating of the separation layer (see 2nd paragraph, page 8).

This claim was rejected on the basis of teachings of the primary references of Sakaguchi and Ahn (see the rejection described above). The reference of Ahn was used primarily to show that the resistivity of GaAs is higher than that of Si. Since the claim limitations do not cite any impurity levels of the two layers and cite only the differences in resistivity, the Applicant's argument (see 3rd paragraph, page 8) that the resistivity of both Si and GaAs varies with the doping level is moot. The reference of Ahn was used to show that the resistivity of GaAs as a compound material is inherently higher than that of elemental Si. The Applicant rightfully agrees that Ahn does teach the Si substrates have lower resistivity when compared to GaAs (see 3rd paragraph, page 8). The method of manufacturing the semiconductor film including the step of preparing the first member including the substrate is taught by Sakaguchi. The Applicant did not argue about Sakaguchi, which was used to reject most of the limitations. For this reason the Examiner believes that Applicant's arguments are not persuasive.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571 272 1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar
Asok K. Sarkar
November 18, 2004

Patent Examiner